Web Results **1 - 10** of about **112** for **"singl -thread" (multi-threading OR multi-thread) verilog** with **Saf search on**. (**0.33** seconds)

Did you mean: "single-thread" (***multithreading OR multithread***) verilog

[PDF] C-slow Retiming of a Microprocessor Core
File Format: PDF/Adobe Acrobat - View as HTML
... Straightforward SMP/**multi-threading** semantics Page 9. ... Page 31. Simple **Multithreading** ... status registers – Alternative: use a **single thread** to handle IO tasks ...
www.cs.berkeley.edu/~yatish/cs252/252slides.pdf - Similar pages

[PPT] C-slow Retiming a Microprocessor Core: Process and Semantics
File Format: Microsoft Powerpoint 97 - View as HTML
... Straightforward SMP/**multi-threading** semantics. C-Slow transformation (1). ... Simple **Multithreading**. ... Alternative: use a **single thread** to handle IO tasks. ...
www.cs.berkeley.edu/~yatish/cs252/252slides.ppt - Similar pages
[More results from www.cs.berkeley.edu]

[PDF] SmartLib Dynamically-Linked SPICE Models
File Format: PDF/Adobe Acrobat - View as HTML
... All models operate in **single thread** and in **multi-thread** parallel mode. ... HSPICE compatibility Page 2. SmartSpice/**Verilog**-A Product Architecture ...
www.silvaco.com/products/analog/ spicemodels/spicemodels_lowres.pdf - Similar pages

[PDF] RAPTOR: A SINGLE CHIP MULTIPROCESSOR
File Format: PDF/Adobe Acrobat - View as HTML
... CMPs use relatively simple **single-thread** processor cores to ... simultaneous points of execution, **multithreading** can be an ... **Verilog** HDL is used for both abstract ...
www.ap-asic.org/1999/proceedings/12-2.pdf - Similar pages

TestBuilder Reference Manual – 3. Concurrency
... A **singl thread** can initiate a transaction and check ... sections that describe the TestBuilder **multithreading** classes and ... in VHDL and always / initial in **Verilog**. ...
www.testbuilder.net/releases/doc/TestBuilder-01.30-s008/ doc/testbuilderref/tbrthreads.html - 101k - Cached - Similar pages

[PDF] No. 1 - Warm 2003
File Format: PDF/Adobe Acrobat - View as HTML
... (One thing **Verilog** does well is to ... and clarity.) I find that most programmers think "**single thread**", but most hard- ware designers think "**multi-thread**". ...
www.cca.org/pm/machine01.pdf - Similar pages

[PDF] GAUTHAM K.DORAI
File Format: PDF/Adobe Acrobat - View as HTML
... C, Java, C++, Perl, Lisp, **Verilog**, Assembly, HTML ... in SMT Processors for High **Singl -Thread** Performance. ... of-order commit in Simultaneous **Multithreading** Processors ...
maggini.eng.umd.edu/users/gauthamt/ publications/resume.softwaredesign.pdf - Similar pages

[PDF] Piranha: Piranha:
File Format: PDF/Adobe Acrobat - View as HTML
... thread 4 Simultaneous **Multithreading** (SMT) SMT superior in **single-thread** performance ... **Verilog** simulation is too slow for comprehensive testing Page 27. ...
research.compaq.com/wrl/projects/ Database/piranha_asilomar.pdf - Similar pages

[PDF] Piranha: A Scalable Architecture Based on Single-Chip ...
File Format: PDF/Adobe Acrobat - View as HTML
... studies have shown that techniques such as simultaneous **multithr ading** (SMT) can ... 9]. While the SMT approach is superior in **singl -thr ad** performance (important ...
www.eecs.harvard.edu/~dbrooks/ cs146-spring2004/piranha.pdf - Similar pages

isdmag.com Articles
... verification languages (HVL) to simulate **V rilog** and VHDL ... academic definition of a **multithr ad** testbench, an ... This **single-thr ad** testbench is basic and easy to ...
newit.gsu.unibel.by/resources/ Journals%5Cisdmag%5Carticles%5C**multithread**.htm - 29k - Cached - Similar pages

Web

Results **1** - **3** of **3** for "multithr aded vhdl" with **Saf search on**. (**0.19** seconds)

Tip: Try removing quotes from your search to get more results.

VAMOS Project Home Page
... VAMOS targets the development of a high performance **multithreaded VHDL** simulator that takes advantage of the availability of multiprocessor hardware and ...
www dafsi.fi.upm.es/~vamos/VAMOS_reg html - 3k - Cached - Similar pages

VIUF Proceedings – FALL 1995
... Style Guidelines for Effective Use of Parallel and **Multithreaded VHDL** Simulators. Willis, John; Paulsen, William; Abstract. The paper ...
www eda org/VIUF_proc/Fall95/abstract_fall95.html - 47k - Cached - Similar pages

VHDL Guideline and Coding Styles
... 290k bytes). Style Guidelines for Effective Use of Parallel and **Multithreaded VHDL** Simulators by Dr. John Willis and Dr. William Paulsen. ...
www.pldworld.com/_hdl/1/rassp. aticorp.org/vhdl/guidelines.html - 9k - Supplemental Result - Cached - Similar pages

Web Results **1 - 10** of about **338** for **vhdl testbench (multi-thr ading OR multi-threaded)** with **Saf s arch on**. (**0.21** seconds)

VHDL WWW Sites
... details about SoftSmith's **VHDL** capture tools, **TestBench** tools, C ... IEEE **VHDL** projects. **Multithreading VHDL** Simulation The paper discusses parallel **VHDL** simulator ...
www.ece.tntech.edu/TechLinks/VHDL_links.htm - 37k - Cached - Similar pages

Pivot Overview
... Automatic access to Verilog/**VHDL** state via ... packages to support **testbench** development (mailboxes ... Interactive debugger (including **multi-threading** debug support). ...
www.greenl.com/Overview.htm - 11k - Cached - Similar pages

Advanced Computer Architecture
... Explain what a **testbench** is used for in **VHDL**. ... between a signal and a variable in **VHDL**? ... mechanisms used in dataflow and **multi-threaded** computer architectures. ...
www-ist.massey.ac.nz/~orjessho/ comp_arch/html/exam98.html - 16k - Cached - Similar pages

VIUF Proceedings -- FALL 1994
... parallel **VHDL** simulator which uses **multithreading** to achieve ... **VHDL** is used to create a working specification ... The specification [**testbench** and models] is expanded ...
www.eda.org/VIUF_proc/Fall94/abstract_fall94.html - 43k - Cached - Similar pages

[PDF] Accellera -SV3.1a approval
File Format: PDF/Adobe Acrobat - View as HTML
... grain process control for **multi-threaded testbench** development ... expressiveness of **t stb nch** infrastructure; random weighted case ... allow a C- or **VHDL**-like approach ...
www.accellera.org/pressroom/ accellera_approves_systemverilog_3_1a.pdf - Similar pages

Processor Architecture Laboratory
... For this purpose, the **multi-threaded** tools (graphical debugger, static lock analyzer and system ... You will do experiments with a **VHDL testbench** that includes a ...
lapwww.epfl.ch/projects/database/list.php?type=semester - 31k - Cached - Similar pages

TestBuilder Reference Manual -- Index
... **multithreading** facility conditions connections $tbv_tbm_connect in Verilog tbv_tbm_connect in **VHDL** TVM instances Verilog example where to put in **testbench** ...
www.testbuilder.net/releases/doc/TestBuilder-01.30-s008/ doc/testbuilderref/testbuilderrefIX.html - 101k - Cached - Similar pages

Annapolis Micro Systems, Inc. - Design and Development
... Development of multi-tasking and **multi-threaded** applications; ... design flow including ASIC specification, **VHDL** design, RTL coding, **testbench** development, code ...
www.annapmicro.com/designanddevelopment.html - 20k - Cached - Similar pages

[PDF] Peer-Based **Multithreaded** Executable Co-Specification
File Format: PDF/Adobe Acrobat - View as HTML
... viewing Verilog always blocks and **VHDL** process statements as ... ends, as specified in the software **testbench**. ... 6. Summary Our unified **multithreading** approach has ...
www.sigda.org/Archives/ProceedingArchives/ Codes/Codes99/papers/1999/codes99/pdffiles/4_5.pdf - Similar pages

AST - EDA - FPGA & ASIC Design
... SPV Software framework for **testbench** automation. ... It works with any Verilog or **VHDL** simulator via a ... for parallel execution that does not use **multithreading**. ...
www.ast.co.il/submenus/fpga_asic_design.php - 16k - Dec 28, 2004 - Cached - Similar pages

Web Results **21 - 26** of about **36** for **vhdl testbench verilog tcl (multi-threading OR multi-threaded)** with **Safesearch on**. (**0.28** seco

DATE 2003 Abstracts
... are: 1. A completely reusable **testbench** that can be ... VLD core) has been described
in **V rilog/VHDL** and implemented ... behavioural models, written in **VHDL**-AMS, each ...
sigda.org/Archives/ProceedingArchives/ Date/papers/2003/date03/htmfiles/sun_sgi/frames/dfabs.htm - 54k - Cached - Similar pages

[PDF] Embedded System Tools Guide
File Format: PDF/Adobe Acrobat - View as HTML
... Rocket I/O, SelectI/O, SelectRAM, SelectRAM+, Silicon Xpresso, Smartguide,
Smart-IP, SmartSearch, SMARTswitch, System ACE, **Testbench** In A ... 122 XMD **Tcl** commands ...
www.scarpaz.com/FPGA/esi_guide.pdf - Similar pages

[PDF] Embedded System Tools Guide
File Format: PDF/Adobe Acrobat - View as HTML
... Rocket I/O, SelectI/O, SelectRAM, SelectRAM+, Silicon Xpresso, Smartguide,
Smart-IP, SmartSearch, SMARTswitch, System ACE, **Testbench** In A ... 103 XMD **Tcl** commands ...
www.hh.se/staff/saag/Xilinx_documentation_bank/ EDK_embedded_system_guide_278.pdf - Supplemental Result - Similar pages

[PDF] System Design Frontier
File Format: PDF/Adobe Acrobat
... nor the test code so that when the HDL and the HDL portion of the **testbench** (the
SCE-MI ... The transport layer uses the standard **Verilog** PLI or **VHDL** FLI for ...
www.hwswworld.com/pdfs/frontier3.pdf - Similar pages

[PDF] System Design Frontier
File Format: PDF/Adobe Acrobat
... This approach is referred to as simultaneous **multithreading** (SMT). ... components and
synthesizable register transfer HDL (SystemC, **VHDL** or **Verilog**) for the ...
www.hwswworld.com/pdfs/frontier1.pdf - Similar pages

[PS] Synthesis of Parallel Hardware Implementations fromSynchronous ...
File Format: Adobe PostScript - View as Text
... emerged as having a distinct advantage in use over the other. As a result,
both **VHDL** and **Verilog** continue to be widely used and sup 15 ...
ptolemy.eecs.berkeley.edu/publications/ papers/98/SDFToParallelVHDL/mwilliamsonThesis.ps - Similar pages

In order to show you the most relevant results, we have omitted some entries very similar to the 26 already displayed.
If you like, you can repeat the search with the omitted results included.

Web

Results **1 - 10** of about **141** for **"vhdl testbench" verilog tcl** with **Safesearch on**. (**0.36** seconds)

VHDL Testbench Creation Using Perl
... for hardware design and verification engineers using VHDL, **Verilog**, SystemC, SystemVerilog, PSL, Perl and **Tcl**/Tk ... **VHDL Testbench** Creation Using Perl. ...
www.doulos.com/knowhow/perl/testbench_creation/ - 11k - Cached - Similar pages

Perl for Hardware Designers
... **Verilog**, SystemC, SystemVerilog, PSL, Perl and **Tcl**/Tk ... translating between related languages: VHDL to **Verilog**, Xilinx Netlist ... **VHDL Testbench** Creation Using Perl. ...
www.doulos.com/knowhow/perl/ - 13k - Cached - Similar pages

www.cadence-europe.com - Education
... several CDN **Tcl** commands and then leverage to build powerful scripts; A lab that takes you through a **VHDL testbench** that instantiates a **Verilog** gate-level ...
www.cadence-europe.com/education/training/course_details.cfm?clO=66 - 35k - Cached - Similar pages

(ESNUG 342 Item 7) ...
... use. (**VHDL testbench** and **Verilog** design). ... it. One of the nicest features of modelsim (**Verilog** or VHDL) is the **TCL** interface. As ...
www.deepchip.com/items/0342-07.html - 16k - Cached - Similar pages

DeepChip Homepage
... We looked at NC-Sim's **Tcl** support, it seemed to be a worthy attempt but not as comprehensive or as ... **VHDL-testbench/Verilog**-netlist for gate level verification. ...
www.deepchip.com/items/dvcon04-02.html - 26k - Cached - Similar pages
[More results from www.deepchip.com]

[PDF] Xilinx - Using the ModelSim FPGA Library Manager - Xcell Issue 35 ...
File Format: PDF/Adobe Acrobat - View as HTML
... Use Browse > Select fpgavendor_xilinx.**tcl** > Open > Next (Please refer ... Choose your HDL language (VHDL or **Verilog**). If you have a **VHDL testbench**, you can run a ...
www.xilinx.com/xcell/xl35/xl35_49.pdf - Similar pages

[PDF] ModelSim Performance and User Interface Key to Success of Siemens ...
File Format: PDF/Adobe Acrobat - View as HTML
... Using the power of **Tcl**/Tk, they were able to design there ... used ModelSim's mixed-language capa- bility to simulate **Verilog** gates and the **VHDL testbench**. ...
www.model.com/news_events/pdf/siemens_success.pdf - Similar pages

FAQ comp.lang.vhdl (part 3): Products & Services
... ch Products: BestBench is a **VHDL testbench** design- and ... we offer: VHDL Language Courses **V rilog** Language Courses ... Design Environment Courses:- PERL and **Tcl**/TK ...
www-online.kek.jp/~yasu/Parallel-CAMAC/vhdl-FAQ3.html - 101k - Cached - Similar pages

Resume of Kenneth E. Martin, Jr., Electrical Design and ...
... Designed VHDL and **Tcl**/Tk utilities to allow VSIM ... commands to be directly executed in a **VHDL testbench**. ... It was originally designed to generate **Verilog** models. ...
home.nc.rr.com/kmartjr/resume.html - 27k - Supplemental Result - Cached - Similar pages

Keith Irwin Resume
... Familiar with C, Vera, **Tcl**, PCI Express, USB, AMBA ... development for B version in **Verilog** and VHDL ... Built bus-functional, procedure based **VHDL testbench** for testing ...
keithirwin.home.comcast.net/3456/ - 97k - Cached - Similar pages